REPORT SD-TR-89-57

Thermal Model for Double-Drift IMPATT Diodes on Diamond Heat Sinks

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31 August 1989

Prepared for

SPACE SYSTEMS DIVISION
AIR FORCE SYSTEMS COMMAND
Los Angeles Air Force Base
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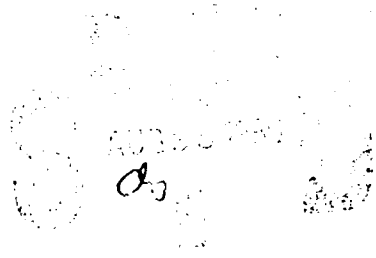

This report was submitted by The Aerospace Corporation, El Segundo, CA 90245, under Contract No. F04701-88-C-0089 with the Space Systems Division, P.O. Box 92960, Los Angeles, CA 90009-2960. It was reviewed and approved for The Aerospace Corporation by M. J. Daugherty, Director, Electronics Research Laboratory.

Lt Steven Boyle was the project officer for the Mission-Oriented Investigation and Experimentation (MOIE) Program.

This report has been reviewed by the Public Affairs Office (PAS) and is releasable to the National Technical Information Service (NTIS). At NTIS, it will be available to the general public, including foreign nationals.

This technical report has been reviewed and is approved for publication. Publication of this report does not constitute Air Force approval of the report's findings or conclusions. It is published only for the exchange and stimulation of ideas.

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UNCLASSIFIED

SECURITY CLASSIFICATION OF THIS PAGE

REPORT DOCUMENTATION PAGE

1a REPORT SECURITY CLASSIFICATION Unclassified	1b RESTRICTIVE MARKINGS
2a SECURITY CLASSIFICATION AUTHORITY	3 DISTRIBUTION / AVAILABILITY OF REPORT Approved for public release; distribution unlimited.
2b DECLASSIFICATION / DOWNGRADING SCHEDULE	
4 PERFORMING ORGANIZATION REPORT NUMBER(S) TR-0089(4925-02)-3	5 MONITORING ORGANIZATION REPORT NUMBER(S) SD-TR-89-57
6a NAME OF PERFORMING ORGANIZATION The Aerospace Corporation Laboratory Operations 6b OFFICE SYMBOL (If applicable)	7a NAME OF MONITORING ORGANIZATION Space Systems Division
6c ADDRESS (City, State, and ZIP Code) El Segundo, CA 90245	7b ADDRESS (City, State, and ZIP Code) Los Angeles Air Force Base Los Angeles, CA 90009-2960
8a NAME OF FUNDING / SPONSORING ORGANIZATION 8b OFFICE SYMBOL (If applicable)	9 PROCUREMENT INSTRUMENT IDENTIFICATION NUMBER F04701-88-C-0089
8c ADDRESS (City, State, and ZIP Code)	10 SOURCE OF FUNDING NUMBERS PROGRAM ELEMENT NO. / PROJECT NO. / TASK NO / WORK UNIT ACCESSION NO.

11 TITLE (Include Security Classification)
THERMAL MODEL FOR DOUBLE-DRIFT IMPATT DIODES ON DIAMOND HEAT SINKS

12 PERSONAL AUTHOR(S)
Csanky, Geza

13a TYPE OF REPORT	13b TIME COVERED FROM ____ TO ____	14 DATE OF REPORT (Year, Month, Day)	15 PAGE COUNT
		1989 August 31	47

16 SUPPLEMENTARY NOTATION

17 COSATI CODES			18 SUBJECT TERMS (Continue on reverse if necessary and identify by block number)
FIELD	GROUP	SUB-GROUP	Diamond heat sink Silicon IMPATT diode Thermal model

19 ABSTRACT (Continue on reverse if necessary and identify by block number)

A thermal model of double-drift IMPATT diodes on diamond heat sinks has been developed. The thermal model approximates the temperature-dependent thermal conductivities of Si and diamond (Type II) by means of simple empirical formulas. The application of the thermal model to three IMPATT diode lots indicates that under life test, junction temperatures are greater than 700°C, while the metal/Si interface temperatures exceed 500°C. An explanation of the failure mechanism is presented. Designs that result in a lower junction temperature are proposed.

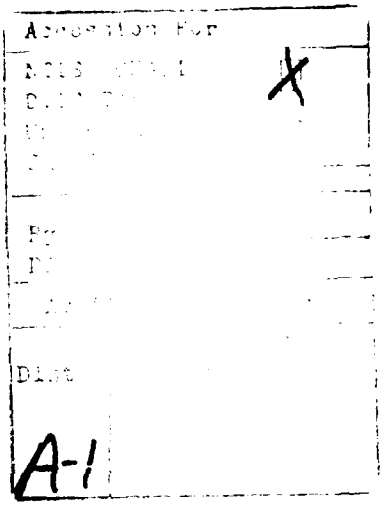
20 DISTRIBUTION / AVAILABILITY OF ABSTRACT	21 ABSTRACT SECURITY CLASSIFICATION	
☒ UNCLASSIFIED/UNLIMITED ☐ SAME AS RPT ☐ DTIC USERS	Unclassified	
22a NAME OF RESPONSIBLE INDIVIDUAL	22b TELEPHONE (Include Area Code)	22c OFFICE SYMBOL

DD FORM 1473, 84 MAR 83 APR edition may be used until exhausted
All other editions are obsolete.

SECURITY CLASSIFICATION OF THIS PAGE
UNCLASSIFIED

PREFACE

I would like to express my appreciation to Drs. C. T. Hoskinson and David Scott of The Aerospace Corporation for their valuable help.



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I. INTRODUCTION

Because IMPATT diodes operate at junction temperatures well in excess of the operating temperatures customary for other semiconductor devices, they frequently fail prematurely as a result of unexpected thermal problems. Therefore, it is important to model IMPATT diodes thermally in order to be able to predict the life expectancy of a device. For this an accurate thermal model is needed, because the normal operating temperatures of IMPATT diodes frequently approach critical levels. Although no model can replicate operating conditions exactly, the best models approximate the true situation accurately enough so that the conclusions drawn by the modeler are valid.

As is well known from elementary physics, when different parts of a body are at different temperatures, heat flows from the hotter parts toward the colder ones. In the case of IMPATT diodes, heat is generated at the p/n junction, so heat flows from the junction toward the heat sink. This flow of heat can occur in several different ways, but in the case of IMPATT diodes the most important method of heat transfer is conduction. By definition, heat conduction is the transfer method by which heat passes through the body itself. The model developed for double-drift IMPATT diodes limits the heat flow to heat conduction and neglects all other heat transfer methods, such as radiation and so on. By limiting heat flow to conduction, one can develop a thermal model based on the thermal resistance. By definition, the thermal resistance θ of any structure can be obtained from the relationship

$$\theta = \Delta T/P \ [K/W] \qquad (1)$$

where ΔT is the rise of temperature due to the dissipated power P, which is converted into heat. Note that θ is the inverse of the thermal conductance.

In this report we develop a thermal model, based on the thermal resistance of the IMPATT structure, that is applicable to double-drift IMPATT diodes. However, prior to the development of the thermal model, it is advantageous to review briefly some important features of IMPATT diodes and the diode structure itself.

II. IMPATT DIODE STRUCTURE

In 1958 W. T. Read[1] predicted that a localized high-field avalanche region followed by a moderately high-field drift region would make an efficient source of microwave energy. It took nearly ten years after Read's paper for silicon (Si) technology to mature to the point that a Read diode structure could be fabricated. The results showed that Read's original predictions were correct, but they also showed that the elaborate outline proposed by Read was unnecessary. Since then, a variety of devices based on Read's principle for generating microwave power have been developed, most recently the double-drift IMPATT diode.

A double-drift IMPATT diode consists of a heavily doped p^+ region followed by a moderately doped p region, a moderately doped n region, and a heavily doped n^+ region. Avalanche breakdown occurs at the p/n junction, while the n^+ and p^+ regions allow ohmic contacts to be made to the IMPATT diode. Figure 1 shows the doping profile of a $p^+/p/n/n^+$ double-drift IMPATT diode, along with the electric field at avalanche breakdown.[2]

During the operation of an IMPATT diode only a relatively small portion of the applied dc power is converted into microwave energy; the rest is converted into heat. The ratio of the microwave energy to the total applied dc power is called the conversion efficiency of the IMPATT diode. To obtain acceptable conversion efficiencies, high current densities are required under avalanche operating conditions; i.e., efficient operation requires large power dissipation. Under continuous operation this power dissipation can be achieved only via structures that are capable of handling the power.

In practical applications there is a specified maximum operating temperature, dictated by reliability considerations, that corresponds to a ΔT_{max}; at the same time, there is a desired conversion efficiency that dictates a minimum current density J_{min}. Because of the ΔT_{max} and the J_{min} requirements, continuous operation can be achieved only by small diode

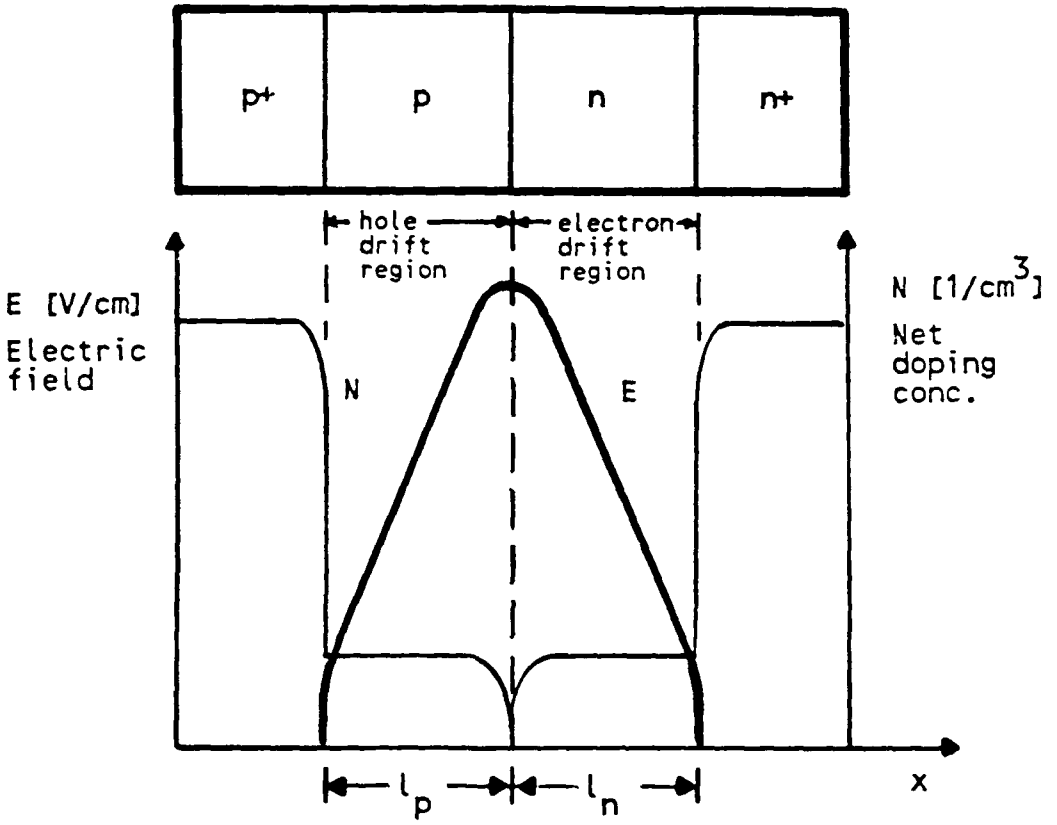

Fig. 1. Cross Section and Electric Field Profile of a Double-Drift IMPATT Diode

chips. Therefore, IMPATT diodes are fabricated by means of a mesa outline having a small chip radius of a <30 μm. An equation defining the maximum chip radius, a_{max}, relative to ΔT_{max} and J_{min} is given later.

To reduce the thermal resistance of the assembly, the IMPATT diode is bonded with its junction side down to a good thermal conductor; this reduces the distance the heat flux must travel from the heat-generating, avalanching p/n junction to the heat sink. In the case of double-drift IMPATT diodes, the heat sink consists of a small cylindrical piece of diamond (Type II) that is hot pressed into a copper (Cu) base. Diamond is used for its excellent heat conductivity, the highest known to date in the temperature range where IMPATT diodes operate. Thinning the n^+ substrate to <25 μm not only reduces the series ohmic resistance but also improves the conversion efficiency of the IMPATT diode.

II. DIODE THERMAL MODEL

The thermal resistance of a single-drift IMPATT structure has been analyzed before. Swan et al.[3] have shown that the total thermal resistance θ_T of a single-drift IMPATT structure can be expressed as the sum of the thermal resistances of the individual components, provided there is an ideal thermal contact between all interfaces. Their analysis is general and therefore applicable to double-drift configurations.

Figure 2 shows a simplified outline of a double-drift Si IMPATT structure mounted on a diamond heat sink; this outline is used to develop the thermal model. Note that the dimensional relationships are distorted. Figure 2 shows that there are two heat-conducting paths, (1) downward toward the heat sink and (2) upward through the top contact. Therefore, the total thermal resistance of the IMPATT structure is the sum of these two and can be expressed as

$$\theta_T = \theta_{down} + \theta_{up} \approx \theta_{down} \ [K/W] \tag{2}$$

The thermal resistance of the upward path has been neglected, since it provides less than 5% of the total heat conduction. Thus the total thermal resistance of the IMPATT diode, θ_T, can be expressed by the thermal resistance toward the heat sink as the sum of four components:

$$\theta_T = \theta_{Si} + \theta_{metal} + \theta_{dia} + \theta_{Cu} \ [K/W] \tag{3}$$

where θ_{Si} is the thermal resistance of the mesa diode, θ_{metal} is the thermal resistance of the metal layer, θ_{dia} is the thermal resistance of the diamond heat sink, and θ_{Cu} is the thermal resistance of the copper base. Consequently, we simplify the development of the thermal model by defining only the components of Eq. (3).

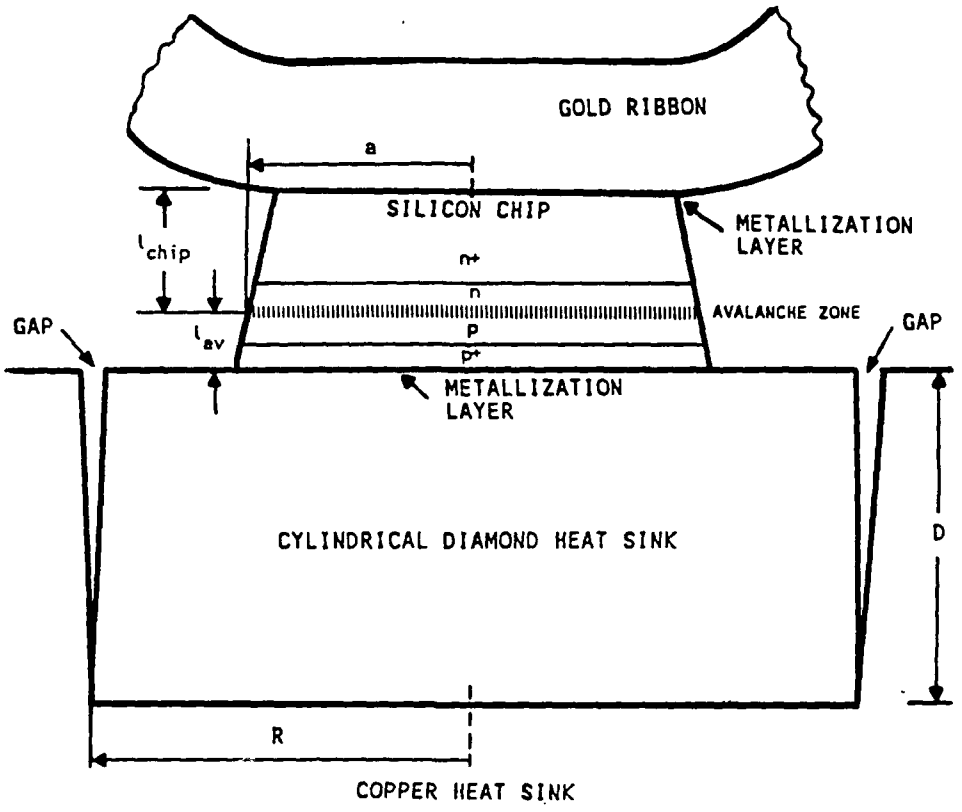

Fig. 2. Diagram of an IMPATT Diode Chip Mounted on a Diamond Heat Sink

Gibbons and Misawa[4] have analyzed the temperature and current distribution of an avalanching p/n junction on a homogeneous semi-infinite heat sink having thermal conductivity k. They used a model in which the diode was represented by a heat flux over a small disc of radius a; the heat flux was incident upon the center of a large cylindrical Cu heat sink. They further assumed adiabatic conditions on the remainder of the top surface. The heat flux was the product of the junction voltage V, which was assumed to be uniform, and the current density J (A/cm^2), which is a function of temperature. They concluded that as the input power is increased, the radial distribution of the current density becomes less uniform while the radial temperature distribution becomes more uniform. A current density of J_{min} results in an approximately uniform heat flux over the disc. Thus the thermal resistance of the Si mesa diode, θ_{Si}, can be represented by a one-dimensional heat-flow model as

$$\theta_{Si} = l_{av}/(k_{Si}\pi a^2) \tag{4}$$

where l_{av} defines the distance between the p/n junction and the heat sink, k_{Si} is the thermal conductivity of Si (a subject we will discuss later), and a is the radius of the mesa diode. Their analysis is general and is applicable to double-drift designs that use diamond heat sinks.

Further, it is assumed that spreading of the heat flux in the thin metal layers of the diamond heat sink is negligible. As a result, when one calculates the thermal resistance of the thin metal layers of the diode chip and the diamond heat sink, the two resistances can be combined and represented by the following one-dimensional heat-flow model:

$$\theta_{metal} = (1/\pi a^2) \sum_{i=1}^{n} l_i/k_i \tag{5}$$

where l_i and k_i represent the thickness and thermal conductivity, respectively, of the various metal layers; n, the number of different metal layers, is usually three, with chromium (Cr), platinum (Pt), and gold (Au)

constituting the three components. These metal layers are applied to both the Si chip (top and bottom) and the diamond heat sink; their thicknesses are given in Table 1.

Table 1. The Thickness of Metalization Layers Applied to Silicon and Diamond Heat Sink

	Metal	Thermal Conductivity, k_i(W/cm K)	Thickness, l_i (μm)
Si Chip	Cr	0.37	0.06
	Pt	0.73	0.20
	Au	3.15	0.70
Diamond Heat Sink	Cr	0.37	0.06
	Pt	0.73	0.035
	Au	3.15	1.00

In a typical assembly the IMPATT die is thermocompression bonded on top of the diamond heat sink, which in turn has been hot pressed into the Cu base. The radius of the diamond heat sink R and its height D are at least ten times larger than the radius of the diode chip a. When the diamond heat sink is hot pressed into the Cu base, the operation leaves a gap between the copper and the side of the diamond heat sink, as shown in Fig. 2. The resulting gap is small, but it causes heat transfer to occur only over the base of the diamond, not over its circumferential face.

To obtain θ_{dia} the heat sink assembly must be considered. The diode is represented by a uniform heat flux that enters the top of the diamond heat sink over a small centrally located area. The radius of the heat flux is equal to the mesa radius a. The heat flux can exit the cylinder only at its other end, since the remaining surfaces are assumed to be insulated. This problem has been analyzed before.[5] Because the radius R and the

height D of the diamond heat sink are much larger than the radius of the diode chip (i.e., R >> a and D >> a), the use of thermal spreading resistance is justified when expressing θ_{dia}. Thus

$$\theta_{dia} = (1/k_{dia}\pi)\,[(1/a) - (1/R)] \tag{6}$$

where k_{dia} is the thermal conductivity of diamond (a subject to be discussed later), and a and R are the radius of the diode chip and the diamond heat sink, respectively.

The final term of Eq. (3) is the thermal resistance of the Cu base. Assuming that the Cu base is large compared to the radius of the diamond cylinder, we can express θ_{Cu} by using the thermal spreading resistance of an infinite half-space. Thus

$$\theta_{Cu} = 1/(4Rk_{Cu}) \tag{7}$$

where k_{Cu} is the thermal conductivity of Cu and R is the radius of the cylindrical diamond heat sink. The model that leads to Eq. (7) assumes that the temperature at the Cu and diamond interface is uniform. This assumption is justified by the solution given by Kennedy[5] and the excellent thermal conductivity of diamond (Type II).

IV. THERMAL CONDUCTIVITY AND THERMAL RESISTANCE OF SILICON AND DIAMOND

Equations (4) and (6) assume that the thermal conductivity of Si and diamond is constant. However, the thermal conductivity of many substances, including Si and diamond, is not constant but varies as a function of temperature. In the temperature range of interest (i.e., the normal operating range of IMPATT diodes, from room temperature to a few hundred degrees Kelvin above room temperature), the thermal conductivity of Si and diamond is an inverse function of temperature:

$$k_{Si} = f(1/T_{Si}) \tag{8}$$

and

$$k_{dia} = f(1/T_{dia}) \tag{9}$$

Figure 3 shows the thermal conductivity, based on actual measured data, of Si, Cu, and diamond (Type II).[6] Note that the thermal conductivity of Cu (as well as all metals) is practically constant in the temperature range of interest.

In calculating the thermal resistance of the Si mesa diode and the diamond (Type II) heat sink, we define the thermal conductivity of Si and diamond by the following empirical formulas:

$$k_{Si} = 292/(T_{Si} - 114) = 292/T_{Se} \tag{10}$$

and

$$k_{dia} = 4000/(T_{dia} - 100) = 4000/T_{de} \tag{11}$$

where T_{Si} and T_{dia} represent the temperatures of Si and diamond in degrees K, respectively, while T_{Se} and T_{de} express effective temperatures.

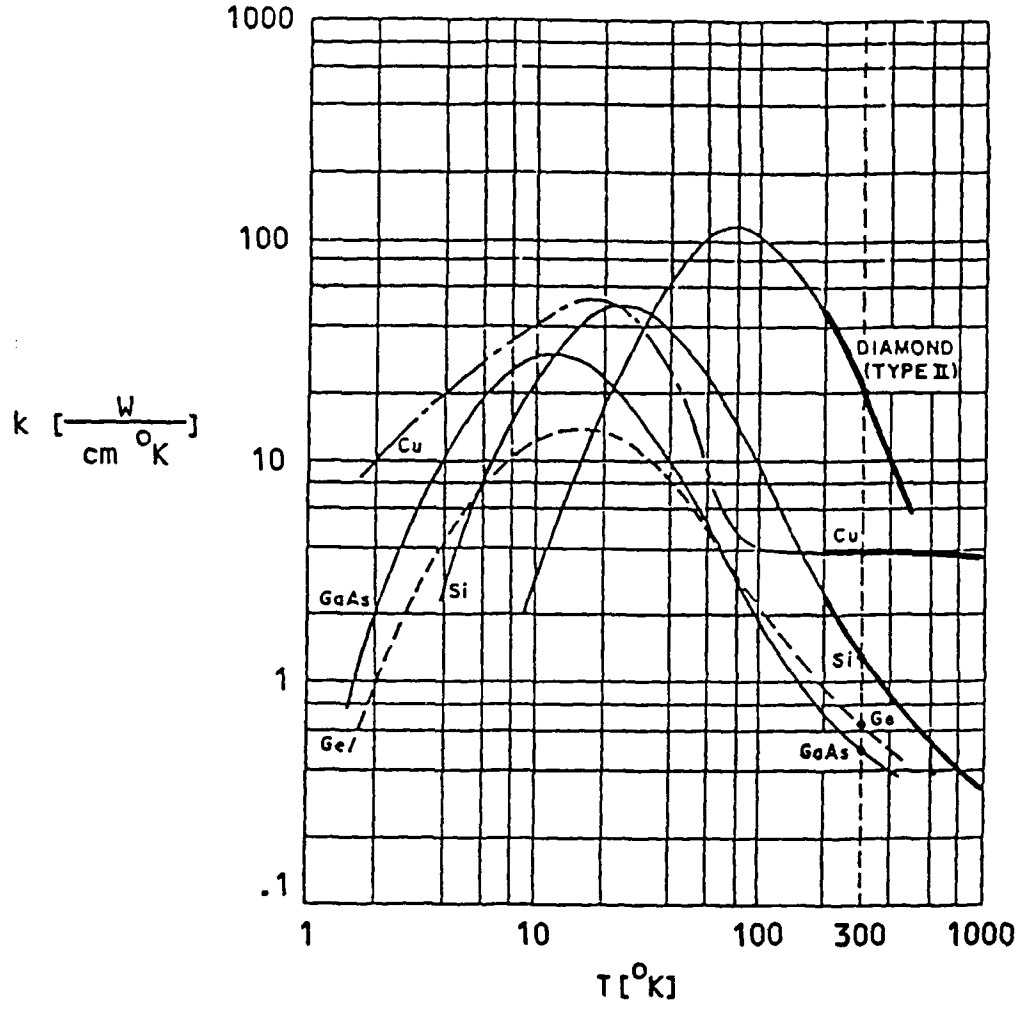

Fig. 3. Thermal Conductivity of Silicon and Diamond (Type II)

Equations (10) and (11) were obtained by fitting the actual curves shown in Fig. 3 at two points each. Comparative plots of the empirical expressions of the thermal conductivity of Si and diamond (Type II) versus the actual measured values are shown in Fig. 4.

Equations (10) and (11) relate the thermal conductivity of Si and diamond to the actual temperatures inside the Si chip and the diamond heat sink, respectively. Unfortunately, during operation the temperature inside the Si chip and the diamond heat sink is not constant; to obtain the true value of θ_{Si} and θ_{dia}, the temperature distribution of the Si chip and the diamond heat sink must be known. As this would be difficult, the use of an approximation simplifies matters greatly. In this approximation it is assumed that θ_{Si} and θ_{dia} can be represented by a thermal resistance that corresponds to the average temperature of Si and diamond.

From Eqs. (4) and (6), θ_{Si} and θ_{dia} can be expressed as

$$\theta_{Si} = (l_{av} T_{Seav})/(292\pi a^2) \tag{12}$$

and

$$\theta_{dia} = (T_{deav}/4000\pi)\,[(1/a) - (1/R)] \tag{13}$$

The average temperature for the Si chip and the diamond heat sink can be obtained from the following approximation:

$$T_{av} = (T_{max} + T_{min})/2 \tag{14}$$

For Si, T_{max} is located at the p/n junction and T_{min} is located at the metal/Si interface. For diamond, T_{max} is located at the metal/diamond interface and T_{min} is located at the diamond/Cu interface. Note that to calculate T_{av}, one must know the interface temperatures.

An easy way to obtain the interface temperatures is to use an equivalent circuit. This is justified because heat conduction is similar

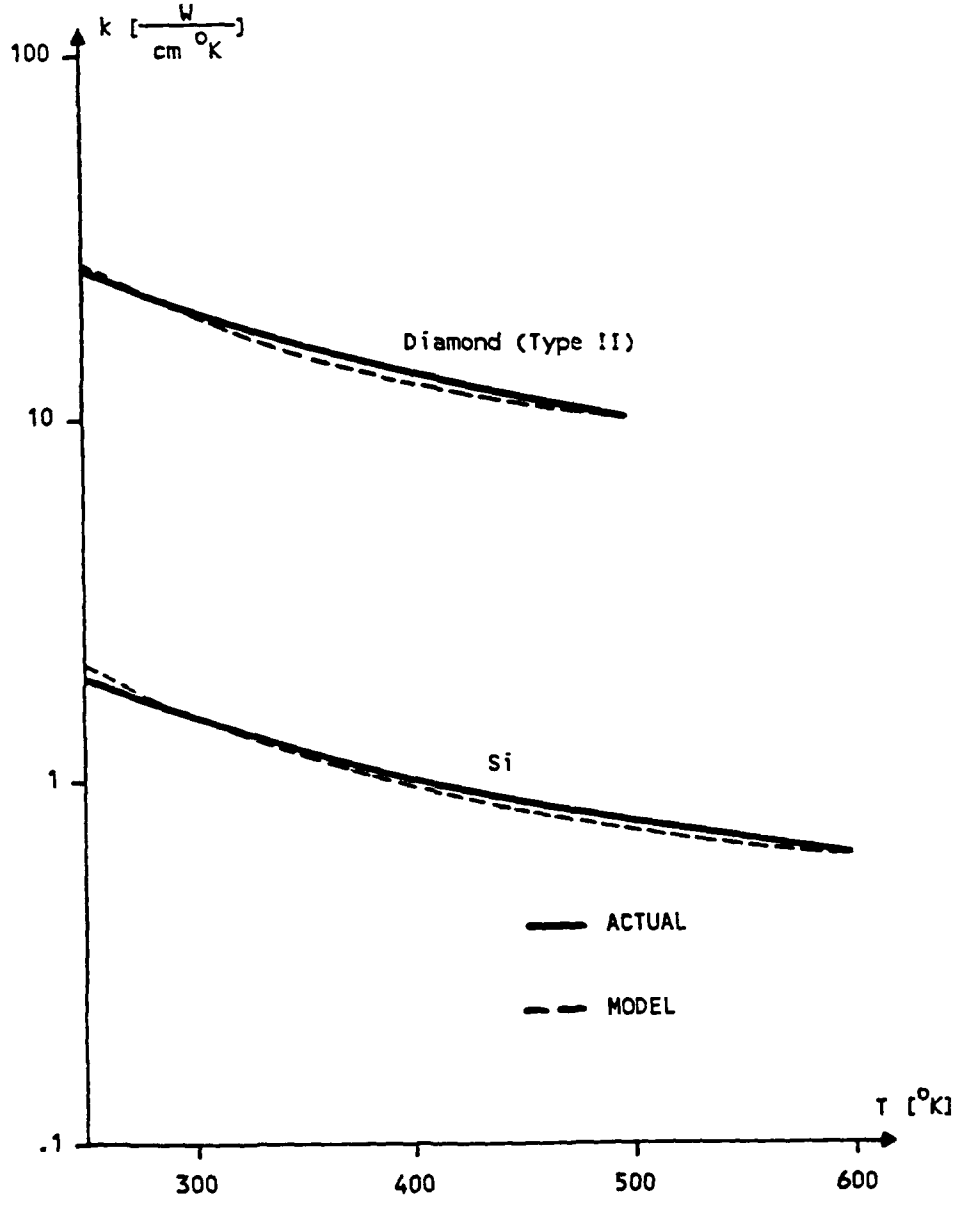

Fig. 4. Comparison of Thermal Conductivity Approximations for Silicon and Diamond (Type II) to Measured Values

to electrical conduction. Note that Eq. (1) is the thermal analog of Ohm's law. Both isothermal and equipotential lines satisfy Laplace's equation. The thermal resistance in degrees centigrade per watt is related by a constant to the electrical resistance in ohms for a given geometrical configuration. The temperature is equivalent to the voltage, while the heat flow is analogous to the current flow. Figure 5 shows the equivalent circuit of the heat flow of an IMPATT diode structure toward the heat sink, i.e., downward; this figure is the electrical representation of Eq. (3). The bottom temperature of Fig. 5 is denoted by T_a, the ambient temperature (T = 293 K), while the top temperature is denoted by $T_a + \Delta T$ (this is also the junction temperature T_j of the IMPATT diode and T_{max} of the Si chip). Thus

$$T_j = T_a + \Delta T \tag{15}$$

The interface temperatures can be obtained by using the equivalent circuit of Fig. 5 as a voltage- or temperature-dividing network. The values of θ_{Si} and θ_{dia} [Eqs. (12) and (13), respectively] can be obtained by using an iterative procedure. From Fig. 5 note that θ_{dia} depends upon θ_{Si} and vice versa. Therefore, both values must be calculated simultaneously.

When the values of θ_{metal}, θ_{Cu}, θ_{Si}, and θ_{dia} from Eqs. (5), (7), (12), and (13), respectively, are entered into Eq. (3), θ_T, the thermal resistance of the IMPATT structure, becomes

$$\theta_T = (l_{av}T_{Seav})/(292\pi a^2) + (1/\pi a^2) \sum_{n=1}^{n} l_i/k_i$$

$$+ (T_{deav}/4000\pi)\,[(1/a) - (1/R] + 1/(4Rk_{Cu}) \tag{16}$$

Equation (16) represents the proposed thermal model of the IMPATT diode.

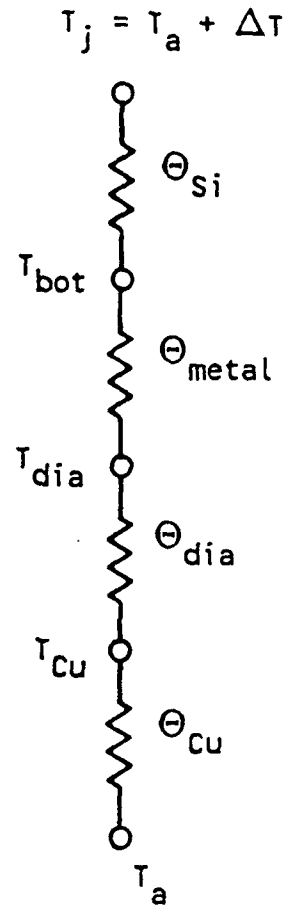

Fig. 5. Equivalent Circuit of the Heat Flow of an IMPATT Diode Structure Toward the Heat Sink (Downward)

V. APPLICATION OF THE THERMAL MODEL

The most important application of the proposed thermal model of the double-drift IMPATT diode is in evaluating accelerated life-test data. The objective of accelerated life testing is to determine the reliability of IMPATT diodes by accelerating thermally activated failure modes. Life-test data are used to estimate the expected life of an IMPATT diode under normal operating conditions. The thermal model as expressed by Eq. (16) is used to define junction temperature, Si/metal interface temperatures, and so on, for three double-drift IMPATT diode lots: DMX 109, DMX 114 and DMX 117. Important conclusions are drawn from the calculations.

Table 2 lists the diode parameters of lots DMX 109, DMX 114, and DMX 117; these parameters are used to calculate the accelerated life-test conditions.

Table 2. Diode Parameters of Lots DMX 109, DMX 114, and DMX 117

Diode Lot No.	DMX 109	DMX 114	DMX 117
Junction Depth, μm (x_{pn})	1.17	0.7	0.72
Doping Concentration, cm^{-3}			
N_A	5.6×10^{16}	9.5×10^{16}	1.2×10^{17}
N_D	7.4×10^{16}	9.7×10^{16}	9×10^{16}
Chip Thickness, μm	15.5	18.2	13.4
l_{chip}, μm	14.33	17.5	12.68
Chip Radius, μm	28.2	25.4	25.5
Breakdown Voltage at 20°C, V	28.59	22.63	22.60
Space-Charge Resistance, Ω	6.51	4.06	4.18

The accelerated life test is performed at elevated temperatures under bias conditions, where the bias is used to generate the heat necessary to obtain the targeted ΔT. Standard life-test conditions are determined by the following method: (1) determine the thermal resistance at room temperature, θ_0, for all diode samples (room temperature is assumed to be 20°C); (2) reverse-bias the sample diodes so that

$$\Delta T_0 = \theta_0 IV \tag{17}$$

is the same for all diodes; (3) start with ΔT_0 = 305°C, then after a predetermined time (~168 hr) successively increase the ΔT_0 to 330, 355, and 380°C or until failure occurs; and (4) record failure times and temperatures for all diodes.

The life-test condition expressed by Eq. (17) uses an artificial junction temperature that is denoted by T_0. T_0 can be expressed as

$$T_0 = T_a + \theta_0 IV = 20 + \theta_0 IV \tag{18}$$

T_0 values used for life tests are 325, 350, 375, and 400°C. Actual junction temperatures are substantially higher than those expressed by T_0.

Failure in a life test usually occurs at the metal/Si interface either at the top or bottom of the IMPATT die. It is important to know the actual interface temperature where failure occurs. Note that because of the temperature drop across the Si layer between the junction and the interface, the temperature at the metal/Si interface is significantly below that at the IMPATT diode junction.

The thermal model as expressed by Eq. (16), together with the equivalent circuit (Fig. 5), will be used to calculate the interface temperatures toward the heat sink of an IMPATT structure under life test.

To calculate the metal/Si interface temperature at the top of the IMPATT die, the equivalent circuit of the upward heat-conduction path must be used. The thermal resistance of the upward heat-conduction path, θ_{up}, can be expressed as

$$\theta_{up} = \theta_{chip} + \theta_{metal} + \theta_{ribbon} + \theta_{ring} \tag{19}$$

where θ_{chip} represents the upward thermal resistance of the Si diode, θ_{metal} is the thermal resistance of the metal layer, θ_{ribbon} is the thermal resistance of the gold bonding ribbon, and θ_{ring} is the thermal resistance of the ceramic or quartz ring used in the assembly. When calculating the value of θ_{chip}, one should use Eq. (4) but should replace l_{av} with l_{chip}. θ_{metal} can be calculated after the data presented in Table 1 are entered into Eq. (5).

The equivalent circuit of Eq. (19) is shown in Fig. 6; note the difference in the temperature values in comparison with those in Fig. 5. The bottom temperature is denoted by $T_{a1} + \Delta T_1$. This is also the junction temperature of the IMPATT diode, which is the same as that expressed in Eq. (15). The top temperature is denoted by T_{a1}. We begin by examining the expression for T_j:

$$T_j = T_{a1} + \Delta T_1 \tag{20}$$

Comparing Eq. (20) to (15), we can see that the ambient temperature and the temperature rise (i.e., T_{a1} and ΔT_1, respectively) are different. The assembly of IMPATT diodes explains this difference.

Figure 7 shows a detailed cross section of the assembly of an IMPATT structure. In assembly a ceramic or quartz ring is bonded on top of the Cu base. A gold ribbon that provides the top contact of the diode is then bonded to the top of the package ring. The inside radius of the ring used in the assembly is 330 μm, while the outside radius is 432 μm. The radius of the diamond heat sink is 380 μm. Therefore, in assembly the ring

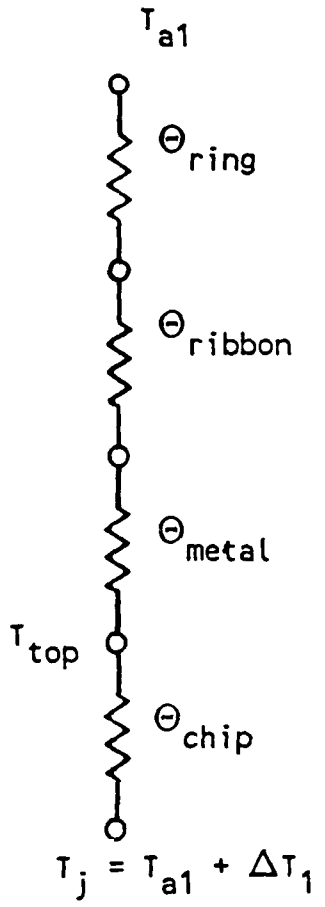

Fig. 6. Equivalent Circuit of the Heat Flow of an IMPATT Diode Structure Through the Chip, the Connecting Ribbon, and the Ring (Upward)

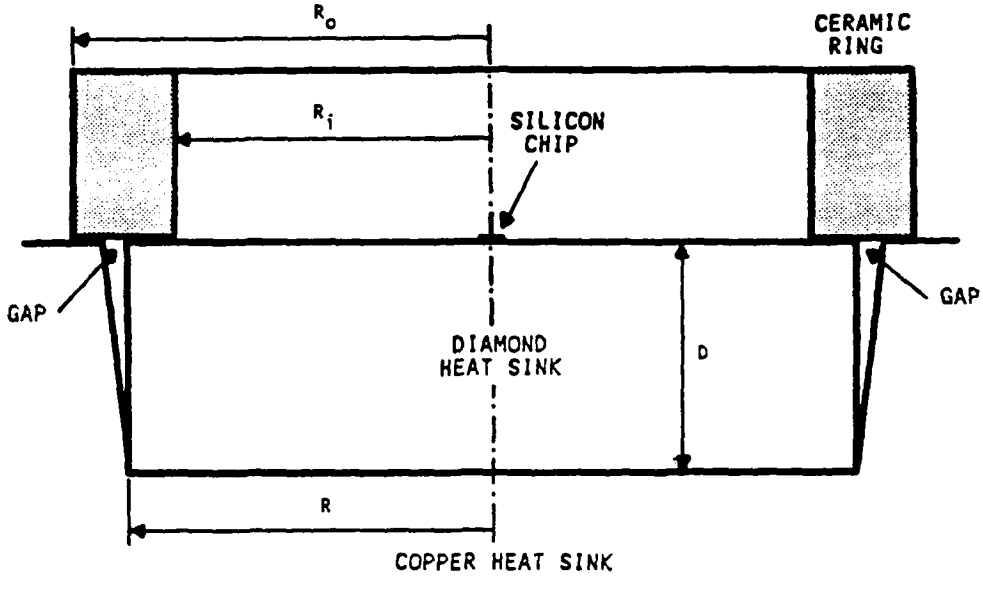

Fig. 7. Diagram of the Package Ring Mounted on Copper Heat Sink. Note the overlap.

overlaps the diamond heat sink and the Cu base, as shown in Fig. 7. As a result, the bottom temperature at the inside of the ring is higher than the bottom temperature at the outside of the ring. The ambient temperature of the upward path, T_{a1}, is the temperature at the bottom of the ceramic ring. This temperature is difficult to define, to say the least, and can only be approximated. The approximation used defines the ambient temperature T_{a1} as the temperature at the interface of the diamond heat sink and the Cu base, instead of room temperature. Because of this difference in the ambient temperature, the temperature rise ΔT_1 must be adjusted accordingly, since there is no change in the actual junction temperature.

Table 3 lists the pertinent dimensions of the three diode lots and the diamond heat sink used to calculate the thermal resistance values.

Table 3. Diode Junction and Diamond Heat Sink Dimensions
(All Measurements are in μm)

Lot No.	Chip Radius	l_{av}	l_{chip}	Diamond Heat Sink Radius	Height
DMX 109	28.2	1.17	14.33	380	250
DMX 114	25.4	0.7	17.5	380	250
DMX 117	25.5	0.72	12.68	380	250

Table 4 gives the component values and the total thermal resistance at room temperature (θ_0) for lots DMX 109, DMX 114, and DMX 117. The values of θ_{Si} and θ_{dia} were calculated by entering data from Table 3 into Eqs. (12) and (13). The value of θ_{metal} was calculated with Eq. (5) and the data shown in Table 1. The value of θ_{Cu} was calculated from k_{Cu} = 3.77 W/cm K.

Table 4. Component Values and Total Thermal Resistance of Lots DMX 109, DMX 114, and DMX 117

	θ_{Si}	θ_{metal}	θ_{dia}	θ_{Cu}	θ_0
DMX 109	0.01604 T_{Seav}	4.75	0.02612 T_{deav}	1.75	14.41
DMX 114	0.01183 T_{Seav}	5.84	0.02924 T_{deav}	1.75	15.34
DMX 117	0.02071 T_{Seav}	5.84	0.02911 T_{deav}	1.75	15.37

The total thermal resistance of an IMPATT structure at elevated temperatures is obtained by calculating the appropriate values of θ_{Si} and θ_{dia}. An iterative procedure is used to define the corresponding values of T_{Seav} and T_{deav} when θ_{Si} and θ_{dia} are calculated. These values, along with the other thermal resistance values stated in Table 4, define the total thermal resistance θ_T of the IMPATT diode structure; this resistance corresponds to a junction temperature. Note that when an IMPATT diode operates or is life tested, then ΔT, the rise in the junction temperature, is given by

$$\Delta T = \theta_T IV \tag{21}$$

where I and V are the diode's bias current and voltage, respectively. The value of θ_0 as given in Table 4 is used to define the accelerated life-test conditions expressed by Eq. (17). Note that if one replaces θ_T with θ_0 in Eq. (21), then ΔT_0 is obtained instead of ΔT. This defines the relationship between the actual junction temperature and the life-test conditions.

To calculate the upward thermal resistance of an IMPATT diode structure, the value of θ_{ribbon} and θ_{ring} must be obtained. In our case the values given by the manufacturer were used: θ_{ribbon} = 305.5 or 299.2°C/W for the ribbon and θ_{ring} = 21.8°C/W for the ceramic package ring.

θ_{Si} was calculated by entering the value of l_{chip} from Table 3 into Eq. (12), and θ_{metal} was calculated from data in Table 1. Table 5 gives the component values and the total upward thermal resistance at room temperature (θ_{Oup}) of lots DMX 109, DMX 114, and DMX 117.

Table 5. Component Values and Total Upward Thermal Resistance of Lots DMX 109, DMX 114, and DMX 117 (in °C/W)

	θ_{chip}	θ_{metal}	θ_{ribbon}	θ_{ring}	θ_{Oup}
DMX 109	0.196 T_{Seav}	1.75	305.5	21.8	364.2
DMX 114	0.296 T_{Seav}	1.75	299.2	21.8	375.7
DMX 117	0.213 T_{Seav}	1.75	305.5	21.8	367.1

To obtain the total upward thermal resistance of the IMPATT structure at life-test temperatures, the formerly mentioned iterative procedure is used to calculate T_{Seav} in order to obtain θ_{Si}. Note that when doing the iterative procedure one must use the ambient temperature T_{a1}; thus the interface temperature of the diamond heat sink and the copper base must be determined beforehand. This value of θ_{Si} and the other thermal resistance values given in Table 5 are then used to obtain the total thermal resistance θ_{up}.

By comparing the value of θ_0 of Table 4 with the value of θ_{Oup} of Table 5, we can see that θ_{up} is indeed much larger than θ_{down}; thus the upward heat-conducting path accounts for less than 5% of the total heat conduction. This justifies the simplifying assumption made before.

After the thermal resistance values were obtained, the temperatures at five different points of the IMPATT diode structure were calculated by means of the electrical circuit analog (Figs. 5 and 6). The five temperatures were at (1) the junction (T_j); (2) the bottom of the Si chip,

at the Si and metal interface (T_{bot}); (3) the top of the diamond heat sink, at the diamond and metal interface (T_{dia}); (4) the interface of the diamond heat sink and the copper base ($T_{Cu} = T_{a1}$); and (5) the top of the Si chip, at the Si and the metal interface (T_{top}). The calculations were performed from T_0 = 100°C to T_0 = 400°C for each lot. Note that the low temperatures of the calculated values correspond to the normal operating temperatures of IMPATT diodes, while the high temperatures correspond to the life-test conditions.

Figure 8 shows a plot of the calculated T_j, T_{bot}, T_{dia}, T_{Cu}, and T_{top} as a function of T_0 for Lot DMX 109. Both scales, the vertical and the horizontal, are in °C. The plot assumes an ambient temperature of 20°C. Figure 8 represents the thermal model of DMX 109. Figures 9 and 10 represent similar plots for Lots DMX 114 and DMX 117, respectively.

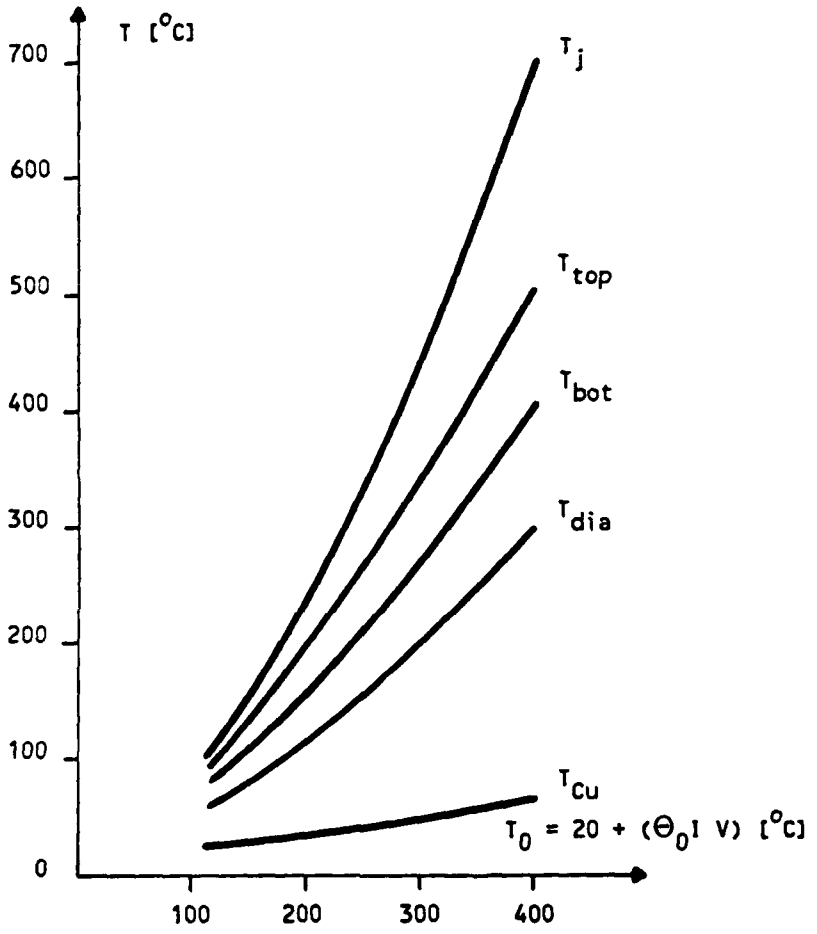

Fig. 8. Plot of the Temperature Values of Lot DMX 109

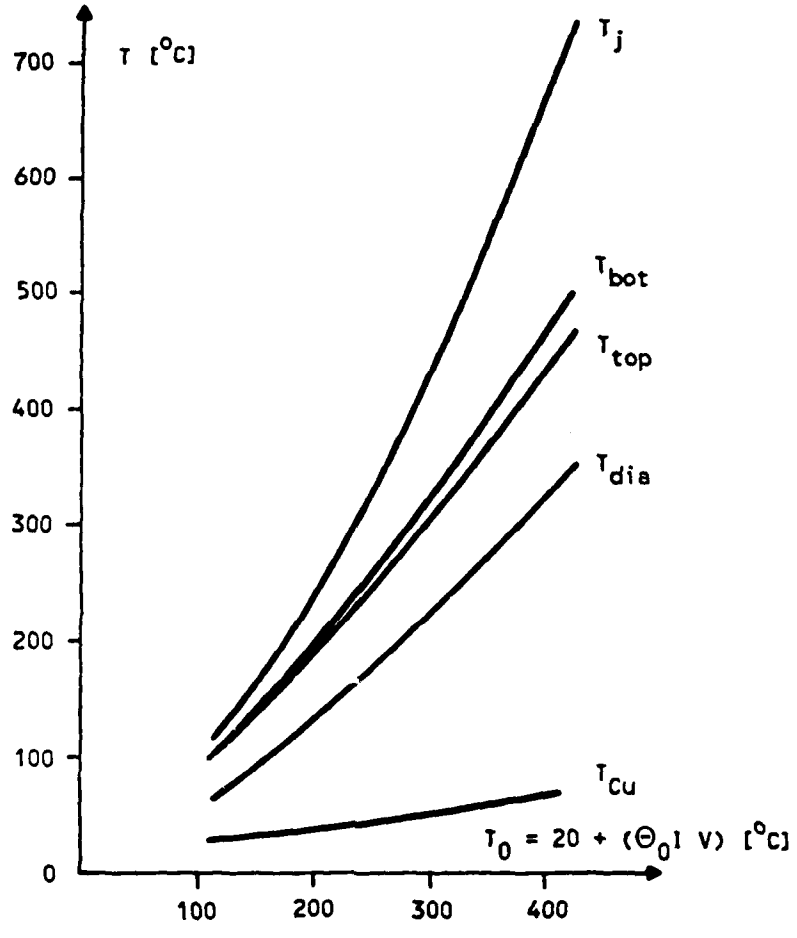

Fig. 9. Plot of the Temperature Values of Lot DMX 114

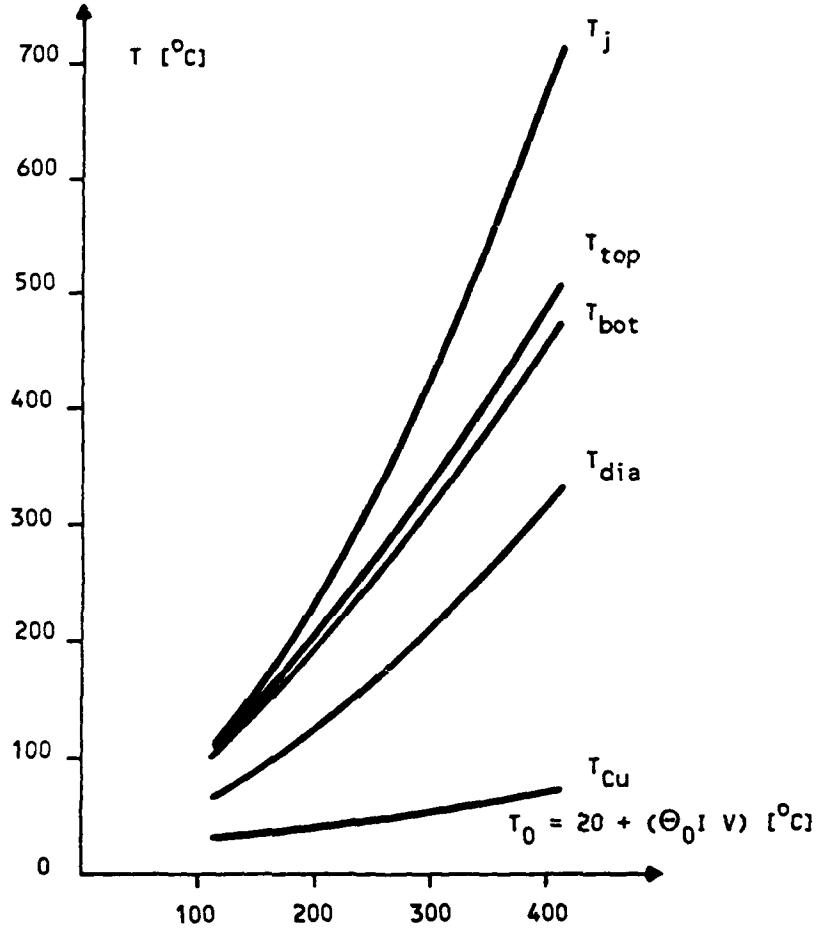

Fig. 10. Plot of the Temperature Values of Lot DMX 117

VI. DISCUSSION

From Figs. 8, 9. and 10 it can be seen that under life-test conditions the junction temperature of IMPATT diodes ranges from about 500°C at T_0 = 325°C to about 700°C at T_0 = 400°C. From the quoted junction temperatures it can easily be concluded that IMPATT diodes are subject to severe thermal stress during life test.

In IMPATT diodes life-test failures usually occur at the metal/Si interface, where temperatures are significantly below the junction temperature. Failure analysis performed on diodes that failed life test indicates that the dominant failure mode is a metal/Si encroachment through the junction, usually near the center of the device. In life test the metal/Si interface temperatures range from a low of about 370°C to a high of greater than 500°C. These temperatures are high, exceeding the Si-Au eutectic temperature (377°C) used as a benchmark. The metal/Si interface temperatures dictate the use of device metalization capable of withstanding temperatures greater than 370°C.

The metalization of an IMPATT diode consists of a chromium/platinum/gold (Cr/Pt/Au) layer, where the Cr layer is in contact with the Si surface. There are three binary interfaces (Cr/Si, Pt/Cr, and Au/Pt) whose properties at elevated temperatures affect the operation of the device.

The Cr/Si phase diagram applicable to the Cr/Si interface indicates that Cr and Si may form several binary compounds, among them Cr_3Si, CrSi, and $CrSi_2$.[7,8] There is little formation of these compounds at temperatures below 600°C. In addition, there is little evidence that Cr enters into solid solution with Si. This means that Cr forms a good barrier in the temperature range of interest for IMPATT diodes and is not the cause of thermal failures.

Cr is also in contact with Pt, and from the Cr/Pt phase diagram it can be seen that Pt dissolves Cr through the formation of CrPt and $CrPt_3$. Of these two compounds, the latter is the more stable. Usually CrPt converts

to $CrPt_3$ at temperatures greater than 400°C. Also, CrPt and $CrPt_3$ are dissolved by Pt. Table 1 shows the usual thicknesses of the various metal layers. It can be seen from this table that, during lifetest, Pt dissolves the Cr layer and eventually the original Cr/Si interface converts to a Pt/Si interface.

The Pt/Si phase diagram indicates that Pt starts forming silicides with Si at low temperatures (~200°C), but accelerated silicide formation occurs at temperatures above 400°C.[9] Furthermore, Pt diffuses rapidly into Si when temperatures exceed 450 to 460°C.[9] From Figs. 8, 9, and 10, note that temperatures exceeding 450°C exist in the bulk of the Si even at the lowest stress temperatures, i.e., where T_0 = 325°C. Therefore, after Cr goes into solid solution with Pt, Pt starts to diffuse into Si. Note also that since the junction of the diode is the hottest part of the IMPATT structure, Pt will congregate to the p/n junction and cause device failures.

The solubility of Au into Pt or vice versa is negligible for temperatures under 600°C. Thus Pt forms a good barrier against Au. The importance of this is that while Si and Au form a eutectic at 377°C, the Pt layer forestalls the Si/Au eutectic formation process even though the metal/Si interface temperatures exceed the Si/Au eutectic temperature. Frequently Pt is replaced by palladium (Pd), but the Cr/Pd and Si/Pd phase diagrams indicate a great similarity between Pd and Pt.

As said before, the objective of life testing IMPATT diodes is to determine the long-term reliability of the devices by accelerating thermally activated failure modes. The failure mode described above is a thermally activated one. However, if valid conclusions are to be reached, three conditions must be met: (1) The failure mode that dominates during life testing must be the dominant failure mode during normal operation. (2) The same failure mode must be the dominant one for every lot. (3) For valid projections to be made, the life expectancy must vary in a known way.

In the case of thermal stress one follows the Arrhenius rule, which says that the expected mean time to failure (MTTF), τ, can be expressed as

$$\tau = \tau_0 \exp(E_A/kT) \tag{22}$$

where τ_0 is a constant, E_A is the activation energy of the thermally induced failure mechanism, k is Boltzman's constant, and T is the absolute temperature. The values of E_A and τ_0 are determined by accelerated life testing. This satisfies condition (3), above.

One can see from Figs. 8, 9, and 10 that during operation or during life test the temperatures at the top and bottom metal/Si interface are not the same. In addition, there is an inconsistency about the location of the hotter metal/Si interface; in the case of lots DMX 109 and DMX 117 it is the top contact, while in the case of lot DMX 114 it is the bottom contact. Since failure originates at the location of the hotter metal/Si interface, thermal failures may originate at either the top or bottom contact. This violates condition (2), since it can be argued that lots DMX 109 and DMX 114 are dominated by different failure modes. For condition (2) to be satisfied, the hotter interface should always be at the same location, say, at the bottom contact.

Using the equivalent circuits shown in Figs. 5 and 6, one can easily calculate the top and bottom interface temperatures. A quick analysis of the problem indicates that if the following condition is satisfied,

$$\theta_{chip}/\theta_{0up} < \theta_{Si}/\theta_0 \tag{23}$$

then the hotter interface will always be located at the bottom of the die. In Eq. (23) θ_{chip} and θ_{Si} represent room-temperature values. We can reduce Eq. (23) to a simple rule of thumb by requiring that

$$l_{chip} > 20\, l_{av} \tag{24}$$

Equation (24) advocates the use of a slightly thicker diode chip than is preferred today, if negative consequences can be minimized. The reason for thinning the wafer is to reduce the series resistance of the n^+ substrate, thereby improving the conversion efficiency of the diode. Adding extra thickness to the wafer, however, may not reduce the conversion efficiency drastically, because the requirement expressed by Eq. (24) would only increase the series resistance of the IMPATT diode from about 5% to less than 8% of the space-charge resistance.

The actual junction temperature T_j of a device during life test exceeds T_0, the temperature defined by the life-test conditions. The reason for this is that the room-temperature values of θ_{Si} and θ_{dia} are used to define T_0. However, θ_{Si} and θ_{dia} are a function of temperature and increase with increasing temperature. Therefore, the thermal resistance of the IMPATT structure at the life-test temperatures, θ_T, is larger than θ_0, resulting in $T_j > T_0$. To reduce the difference between T_j and T_0, the values of θ_{Si} and θ_{dia} must be kept small.

In addition to being a function of temperature, θ_{Si} is also a function of the physical dimensions of the diode chip. It is directly proportional to l_{av}, the thickness of the Si layer between the junction and the heat sink, and it is inversely proportional to a, the diameter of the mesa diode. To obtain as small a value of θ_{Si} as possible, the diode must have a minimum l_{av} and a maximum a.

When operating as a microwave source, the IMPATT diode exhibits a negative ac resistance; i.e., there is a phase shift of π between the voltage and current waveforms. A phase shift of $\pi/2$ is created by the avalanching junction and a phase shift of $\pi/2$ is created by the drift of the carriers. The width of the drift region is an inverse function of the frequency; i.e., it becomes smaller with increasing frequency. In double-drift IMPATT diodes, the drift region extends to both sides of the p/n junction; as a result there is a relatively thick layer of Si between the junction and the heat sink.

Since l_{av} is determined by the thickness of the epitaxial layer, it is constant for every diode fabricated from a given Si wafer. While l_{av} is the same for every diode in a lot, the radius a of individual devices within a lot varies considerably as a result of a final trim-etch processing step. This means that for a diode lot the radius a of a diode chip becomes an important parameter when calculating θ_{Si}. Figure 11 shows a normalized plot of θ_{Si}/T_{Seav} (normalized to l_{av} = 1 μm) as a function of a. Note that the plot of Fig. 11 is independent of temperature. Since the radius of a diode chip is usually 20 to 30 μm, a small variation in a results in a large variation in θ_{Si}.

It can be shown that the maximum radius of an IMPATT diode chip, a_{max}, is a function of the heat sink used and can be expressed as

$$a_{max} = (\Delta T_{max} k_{hs})/(V_{op} J_{min}) \qquad (25)$$

where ΔT_{max} is the maximum rise of T_J allowed, k_{hs} is the thermal conductivity of the heat sink, V_{op} is the operating voltage, and J_{min} is the minimum current density needed for acceptable conversion efficiency. Equation (25) demonstrates the need for a heat sink to have excellent thermal conductivity and a large ΔT_{max} (large T_J).

The use of a diamond/copper heat sink has the effect of increasing the thermal conductivity of the heat sink. To calculate the thermal resistance of a heat sink, an expression for thermal spreading resistance is used. The thermal spreading resistance of a heat sink is a function of the radius of the diode chip and the thermal conductivity of the heat sink. Figure 12 shows the difference between the thermal spreading resistance of a copper or a diamond/copper heat sink. The solid line shows the thermal spreading resistance of a copper heat sink as a function of the radius of the IMPATT die, while the dotted lines show the combined thermal spreading resistance of a diamond/copper heat sink as a function of the die radius at a diamond temperature of 373 K (100°C) and 573 K (300°C), respectively, using a diamond chip having a radius of 380 μm. The 373 K diamond temperature

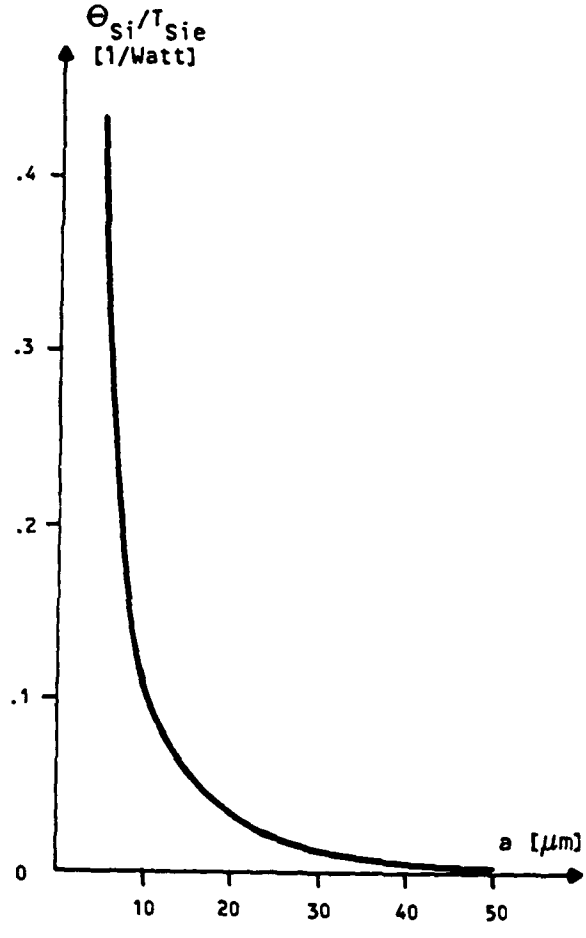

Fig. 11. Plot of θ_{Si}/T_{Seav} as a Function of Chip Radius a

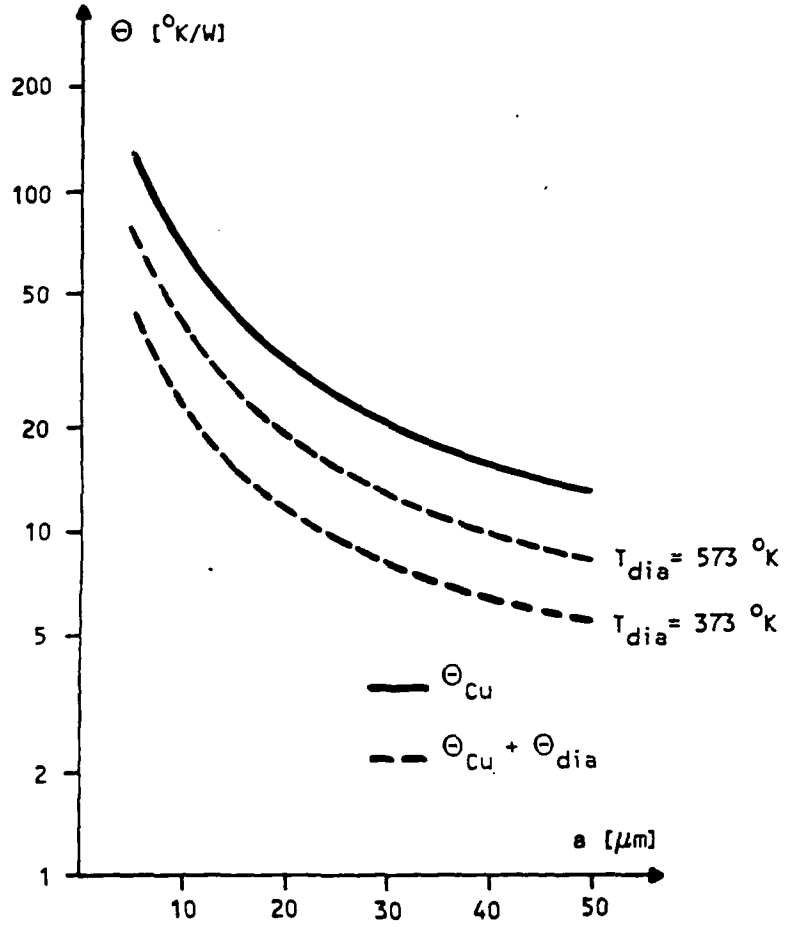

Fig. 12. Plot of the Thermal Spreading Resistance of Copper Heat Sink and Diamond/Copper Heat Sink as a Function of Chip Radius a

corresponds to standard operating temperature, while the 573 K diamond temperature occurs during life test. Figure 12 demonstrates the advantage of using diamond heat sinks.

Finally, the implementation of a minimum l_{av} and a maximum a leads to the lowest possible junction temperature and the lowest metal/Si interface temperatures.

VII. CONCLUSIONS

We have developed a thermal model of double-drift IMPATT diodes on a diamond heat sink by using empirical formulas [Eqs. (10) and (11)] that closely approximate the thermal conductivity of Si and diamond (Type II).

An application of this thermal model to three IMPATT diode lots under life test indicates that extreme junction temperatures, in excess of 700°C, are reached; these temperatures are higher than those predicted by former thermal models. In the three diode lots modeled, the temperatures at the metal/Si interface exceeded the benchmark Au/Si eutectic temperature (377°C). It was found that at these elevated temperatures the diffusion of Pt into Si is the cause of thermal failures.

The existence of such extreme junction temperatures during life test is the result of the method by which the life-test conditions are defined. Under life test the IMPATT diode is subject to extreme stress. In order to reduce the temperature stress to a more acceptable value, the IMPATT die must have a minimum l_{av} and a maximum a. Unfortunately, there are limits on both of these parameters.

Our thermal model also indicates a need to reevaluate the life-test results of IMPATT diodes. Prior thermal models that were used to determine T when calculating τ_0 and E_A underestimated the actual junction temperature during life test. Therefore, by using the thermal model developed here, one should correct the life expectancy of IMPATT diodes to reflect these changes.

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